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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/965,913	09/28/2001	Jerome J. Johnson	COMP:0241 P01-3647	4231

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Michael G. Fletcher
Fletcher, Yoder & Van Someren
P.O. Box 692289
Houston, TX 77269-2289

EXAMINER

MOAZZAMI, NASSER G

ART UNIT	PAPER NUMBER
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2187

DATE MAILED: 02/13/2004

8

Please find below and/or attached an Office communication concerning this application or proceeding.

pre

Office Action Summary

Application No.

09/965,913

Applicant(s)

JOHNSON ET AL.

Examiner

Nasser G Moazzami

Art Unit

2187

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 12 January 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-19 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-19 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. This office action is in response to applicant's amendment dated 01/12/2004 in response to office action mailed on 10/06/2003.

Response to Arguments

2. Applicant's arguments with respect to the rejected claims have been considered, but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

4. Claims 1-2, and 9-10 are rejected under 35 U.S.C. 102(e) as being anticipated by Cho et al., hereinafter Cho and claims 1-2 are rejected under 35 U.S.C. 102(e) as being anticipated by Van Hook et al., hereinafter Van (U.S. Patent No. 6,564,304).

As for claims 1-2, Cho teaches a memory system and method of processing a read request comprising the acts of: transmitting a first read request from a requesting device, the first read request comprising a first system address **[transactions from the one of the devices (column 1, lines 12-13)]**; receiving the first read request at a memory controller **[memory controller receiving an access request]**; mapping the first system address into a first memory address, the first memory address comprising a first chip select, first bank address, a first row address and a first column address **[first portion of the address is a row address, the second portion of the address is a column address (column 1, lines 19-21); memory controller may provide a separate select signal (column 1, lines 26-29); portion of the address is used to select a bank (column 2, lines 44-45)]**; sorting the first read request by one of the first chip select and the first bank address such that the first read request is injected into a first read queue **[transaction queue 30 issues the transactions to one of the channel control circuits 32A-32B (column 7, lines 6-8; also see Fig. 2)]**.

As for claims 9-10, Cho discloses that the chip select identifies a corresponding DIMM to which the request is directed **[by asserting the chip select, the corresponding DIMM is selected (column 7, lines 47-49)]** and bank address identifies a corresponding bank in a corresponding DIMM to which the request is directed **[selecting a bank within the SDRAMs within the selected DIMM (column 8, lines 9-10)]**.

As for claims 1-2, Van teaches a memory system and method of processing a read request comprising the acts of: transmitting a first and second read requests from a requesting device, the first and second read requests comprising a first and second system addresses **[request from one of the memory master M0-M4 (see Fig. 1)]**; receiving the first and second read requests at a memory controller **[memory controller 105 (column 4, lines 65)]**; mapping the first and second system addresses into a first and second memory addresses, the first and second memory addresses comprising first and second chip selects, first and second bank addresses, first and second row addresses and first and second column addresses **[inherent in the art, because a bank address in addition to a row and column addresses is needed to specify a memory location; for inherency support, please see patent numbers 6,470,433 and 5,367,669]**; sorting the first and second read requests by one of the first and second chip selects and the first and second bank addresses such that the first and second read requests in injected into a first and second read queues **[the requests from the RQ0-RQ4 are placed into sort queue 101 (odd or even 102 and 103)]**.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Art Unit: 2187

6. Claims 2-8, and 11-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cho or Van in view of Tran et al., hereinafter Tran (U.S. Patent No. 6,598,132).

As for claims 3-8, and 11-19, Cho and Van disclose the claimed invention, including that the second chip select identifies a corresponding DIMM to which the second request is directed and a second bank address identifies a corresponding bank in a corresponding DIMM to which the second request is directed **[by asserting the chip select, the corresponding DIMM is selected (column 7, lines 47-49); selecting a bank within the SDRAMs within the selected DIMM (column 8, lines 9-10); and a plurality of SDRAM [see column 7, lines 38-40], however Cho or Van fails to specifically teach alternating the read requests from the first and second queues, so that back-to back requests are processed between the first and second queues and back-to back request are not processed to the same bank.**

Tran discloses a buffer memory, a buffer manager and a queue manager. Tran further discloses a SDRAM including number of banks and an order in which the buffer manager read and writes to the various banks. Furthermore Tran discloses that back-to-back read are not processed for the same bank, since each bank requires additional cycles to recover after a read access, so that it would be advantageous to not process back-to-back read requests to the same bank in order to have time to precharge the bank for the next access **[column 6, lines 34-65].**

Art Unit: 2187

Accordingly, it would have been obvious to one having ordinary skill in the art at the time of the current invention to use bank accesses as being taught by Tran into Cho and Van memory system in order to have time to precharge the bank for the next access.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

U.S. Patent No. 6,539,487 (Fields, Jr. et al.)

U.S. Patent No. 6,470,433 (Prouty et al.)


U.S. Patent No. 6,301,299 (Sita et al.)

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nasser G Moazzami whose telephone number is (703) 305-0017. The examiner can normally be reached on 7:00AM-5:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks can be reached on (703) 308-1756. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Art Unit: 2187

9. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).


Nasser Moazzami
02/11/2004